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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,432	09/30/2003	Allen Bruce Goodrich	1001.29	6197

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EXAMINER	
DARE, RYAN A	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,432	GOODRICH, ALLEN BRUCE	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 21-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Maiyuran et al., US Patent 6,485,432.

3. With respect to claim 21, Maiyuran teaches an apparatus for a Y-way set-associative cache memory (e.g. 32) having Y>1 blocks and X>1 sets, wherein each block y, 0<=y<=(Y-1), or each set x, O<=x<=(X-1), is adapted to store an address tag (e.g. Tag), a state (e.g. State) and Z words (e.g., W), O<=z<=(Z-1), the apparatus comprising:

first circuitry adapted to receive a fetch address, determine a set associated with the fetch address, read Y address tags and Y states corresponding to the associated set, determine which of the Y address tags are valid based on the Y states, compare the fetch address to one or more valid address tags, and generate, if oe of the valid address tags matches the fetch address, a first control signal indicating that the block associated with the valid address tag is a matching block, in col. 4, lines 1-12;

second circuitry (e.g. 132, 138 a-d, and 134a-d) adapted to receive the fetch address, receive the first control signal generated by the first circuitry, generate a second control signal (e.g., 126e) based on the first control signal and indicating the matching block, generate block-enable control signals (e.g., 126a-d) for the cache memory, apply the block-enable control signals to the cache memory, such that the matching block in the cache memory is enabled and the (Y-1) other blocks in the cache memory are at least partly disabled, and apply the fetch address to the cache memory to read one or more associated words from the enabled matching block, in col. 4, lines 21-24

third circuitry (e.g., 112) connected to an output of each block of the cache memory and adapted to receive the second control signal generated by the second circuitry, receive the one or more associated words from the enabled matching block, and select one or more associated words for output from the cache memory based on the second control signal, in col. 2, lines 47-50.

4. With respect to claim 22, Maiyuran teaches the invention of claim 21, wherein power consumed by each of the (Y-1) at least partly disabled blocks is less than the power consumed by the enabled, matching bock, in col. 1, line 65 through col. 2, line 5.

5. With respect to claim 23, Maiyuran teaches the invention of claim 21, wherein:

during a clock cycle k:

the first circuitry receives the fetch address, determines the associated set, reads the y address tags and the Y states corresponding to the associated set, determines the

one or more valid address tags, compares the fetch address to the one or more valid address tags, and generates the first control signal, in col. 9, lines 38-45; and

the second circuitry receives the fetch address, receives the first control signal, and generates the block-enable control signals, in col. 10, lines 9-30; and

during a next cycle k+1:

the second circuitry generates the second control signal, applies the block-enable control signals to the cache memory to enable the matching block and at least partly disable the (y-1) other blocks and applies the fetch address to the cache memory to read the one or more associated words from the enabled matching block, in col. 10, lines 9-30; and

the third circuitry receives the second control signal, receives the one or more associated words form the enabled matching block, and selects the one or more associated words for output from the cache memory based on the second control signal, in col. 1, lines 9-30.

6. With respect to claim 24, Maiyuran teaches the invention of claim 21, wherein:

the first circuitry comprises a first latch adapted to latch the fetch address, in col. 9, lines 38-45;

the second circuitry comprises:

a second latch adapted to latch the first control signal and output the second control signal, in col. 9, lines 38-45; and

the third circuitry comprises a multiplexer adapted to receive the outputs form the blocks and select the one or more associated words from the enabled matching block based on the second control signal from the second latch, in col. 10, lines 9-30.

7. Claims 25-28 claim a method that is similar to claims 21-24 and are therefore rejected using similar logic.

8. Claims 29-32 claim a cache memory that is similar to claims 21-24 and are therefore rejected using similar logic.

Response to Arguments

9. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar memory power reduction systems.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ryan Dare/
Ryan Dare
August 6, 2007

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
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